# Point-on-Wave Switching of Capacitor Banks

An overview of the theory and a presentation of an installed system with obtained results.

The latest Engineering Recommendation (EREC) P28 issue 2 makes specific reference to the switching of capacitor banks, and the subsequent voltage disturbances this may cause. Furthermore, there are certain Grid Code connection conditions that call for reactive compensation measures to have the ability to be switched in and out at higher frequency than would normally be possible. Due to this, the application of Point-on-Wave switching with capacitor banks is particularly relevant.

## Theory

When a capacitor bank is energised there is commonly a large and high frequency inrush current spike. This inrush current can lead to a voltage increase at the PCC. The magnitude and frequency of the voltage rise depends on the inrush current, network fault level and X/R ratio. Furthermore, when a capacitor bank is de-energised a residual DC voltage will be left on the capacitors. This commonly means there must be a 6-10 minute delay period while the voltage decays before the bank can be re-energised.

When switching capacitors, inrush current occurs when there is a rapid change of voltage across the capacitors. The theory of Point-on-Wave switching applied to capacitors is to ensure that this voltage change is avoided, or at least kept to an absolute minimum. When a capacitor bank is de-energised and completely discharged, there is 0V across the capacitors, so for this state POW aims to switch the phases at 0V. Conversely, when the capacitor bank is de-energised and fully charged, there is maximum voltage across the capacitors, for this state POW aims to switch the phases at peak voltage. Finally, for a discharging capacitor bank, POW aims to target the voltage that remains on the capacitors, until it reaches a fully discharged state and once again targets 0V.

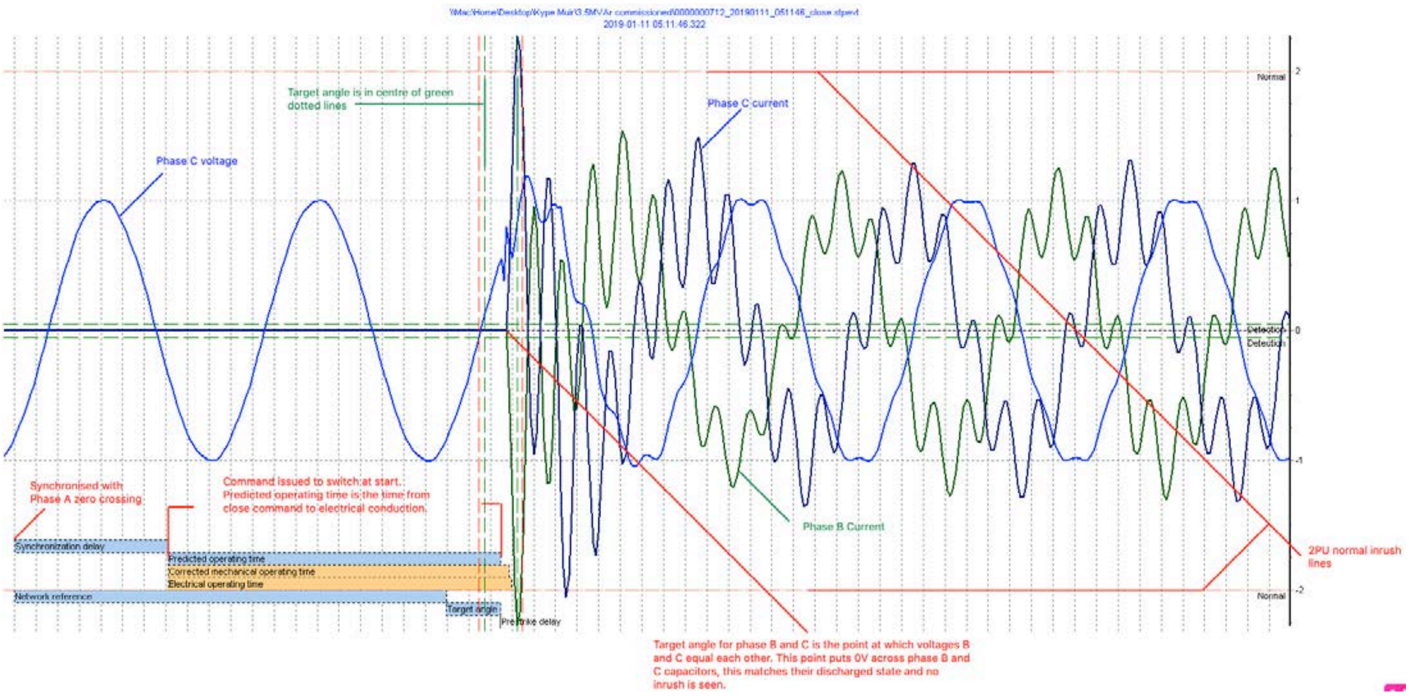


Figure 1 - Discharged Capacitor Bank - Phase B and C close

The above waveform is a closing event on a discharged capacitor bank for phases B and C. These are the phases that are energised first. As can be seen above, the SynchroTeq targets the point that phase B and C voltages cross, resulting in zero volts across phase B and C capacitors and minimum inrush current.

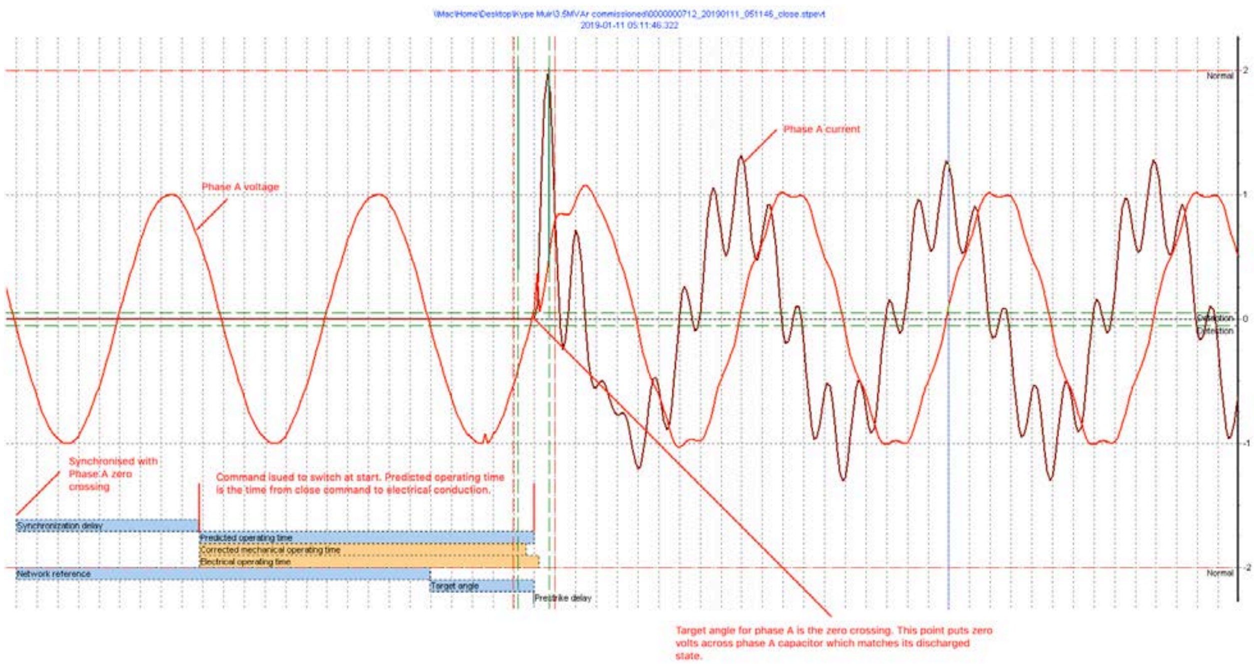


Figure 2 - Discharged Capacitor Bank - Phase A close

The above waveform is a closing event on a discharged capacitor bank for phase A. This phase is energised last. As can be seen above, the SynchroTeq targets the point that phase A voltages crosses 0V, resulting in zero volts across the capacitors and minimum inrush current. The SynchroTeq operates identically for a fully or partially discharged capacitor banks, the only difference is the target angle and thus voltage.

## Wind Farm Application

Enspec have manufactured and supplied a number of Point-on-Wave switched capacitor bank systems to Wind Farms across the UK. One of these included a 6MVAr and a 3.5MVAr de-tuned capacitor bank. Originally the site was planned to include a full STATCOM system for the reactive compliance of the site, but instead the design was changed to use the rapid reactive response of the turbines in conjunction with fast switched capacitor banks. This greatly lowered the capital cost of the reactive compensation system. Below is a comparison of capacitor bank switching at this site with and without the Point-on-Wave system enabled.

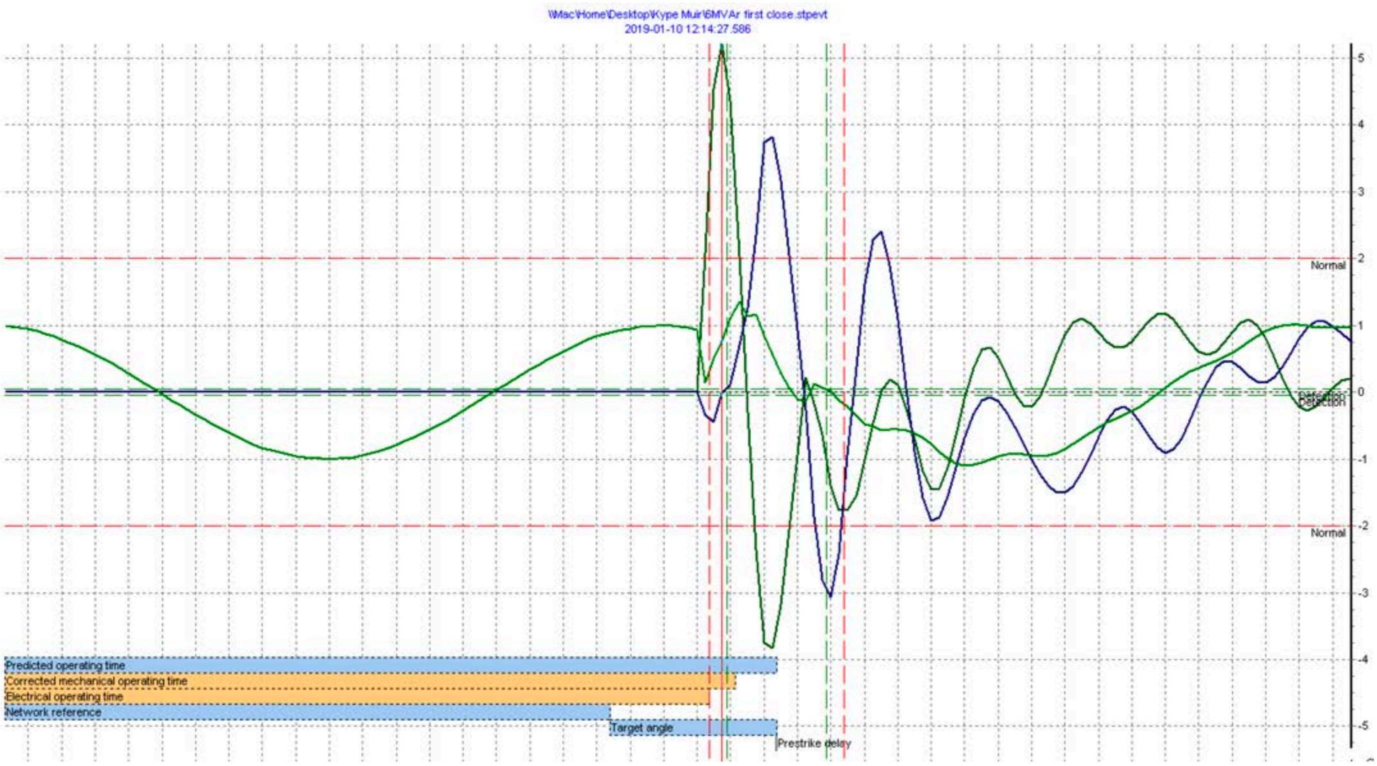


Figure 3 - Capacitor Bank Energisation without PoW

The above shows a closing operation without the PoW system enabled. This resulted in inrush currents of 6pu at the moment of energisation. It should be noted that these banks were de-tuned in order to avoid harmonic resonance. These series de-tuning reactors provide an amount of inrush current damping and so closing events on standard capacitor banks can lead to inrush currents greater than 20pu.

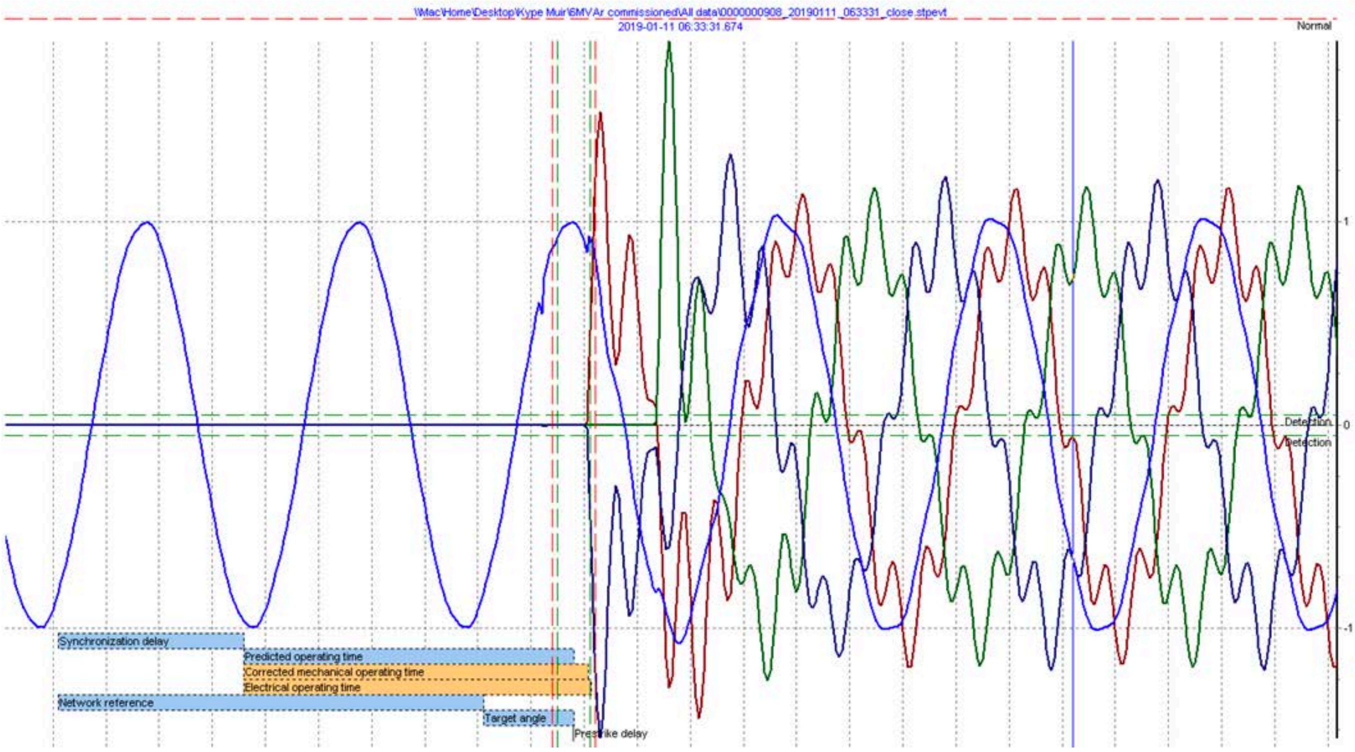


Figure 4 - Capacitor Bank Energisation with PoW

The above shows a closing operation with PoW. This was also a fast re-energisation, with the previous de-energisation occurring only 10 seconds before. This. Resulted in greatly reduced inrush currents of 1.5pu and will have caused a much smaller voltage disturbance at the site PCC. The distorted current waveform that is shown above is completely expected for this system – the capacitor banks were de-tuned and designed to absorb the sites $7^{th}$ harmonic current.



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